A signal KS1 present on the channel is supplied to an inverting Schmitt trigger ST11, whose output signal SST11 is supplied via a NAND gate NA21 to the reset input R of the D-type flipflop DF11. If the signal KS1 rises above a threshold value prescribed by the Schmitt trigger ST11, then the output signal SST11 from the Schmitt trigger ST11 assumes a low level and resets the flipflop DF11 via the NAND gate NA21, as a result of which the level at the flipflop's noninverting output QP falls to a low level. When the high pulse produced at the output QP of the flipflop is generated, use is made of the fact that, particularly during signal transmission via a channel which contains an inductive transformer, the potential on the channel follows the pulse PS1 only after a time delay, which means that the D-type flipflop DF11 is not reset until after this delay time, which determines the duration of the pulse. The duration of the pulse after a rising edge of the input signal Sin is thus prescribed by the channel properties and possibly by the delay times of the logic components. In this way, the pulse length of the transmission pulse PS1 and hence the power consumption are automatically minimized. Delay times for the logic components are incidentally taken into account in the illustration shown in Fig. 1 only where they are necessary for the operation of the circuit arrangement.